ABSTRACT

The present invention describes methods, apparatus, and systems related to polysilicon gate contact openings over active regions formed by a separate mask to provide enough control of dielectric removal to produce a contact opening at least down to the gate layer but not down to the junction layers. Embodiments include, self-aligned polysilicon contacts done by timed contact etch, by a two layer dielectric, by adding a dielectric etch stop layer, and by partially planarizing a dielectric or etch stop layer over the gate layer. Thus, even if mis-aligned, the gate contact openings will be deep enough to reach active region gates, but not deep enough to reach junctions. As a result, by using a separate mask and by selecting a period of time for etching to active gates, gate contact openings can be formed during manufacture of ICs, semiconductors, MOS memory cells, SRAM, flash memory, and various other memory cells.